ABSTRACT

A semiconductor device including: a cell transistor including: a pair of source and drain regions formed in a surface portion of a silicon substrate so as to have a predetermined space therebetween; a channel region sandwiched by the source and drain regions; a gate formed above the channel region with a gate dielectric film being formed therebetween; and a silicon plug formed on the silicon substrate, the silicon plug electrically contacting the source and drain regions, an upper portion of the silicon plug being a first self-aligned silicide portion.